Timing requirements, from LHC hardware commissioning to beam operation

J.Lewis

This talk

- Overview
  - Central timing
  - Timing reception
- The Hardware

Slides 3..9 Mostly Old Stuff

- Requirements for LHC filling

Slides 9..19 New Stuff

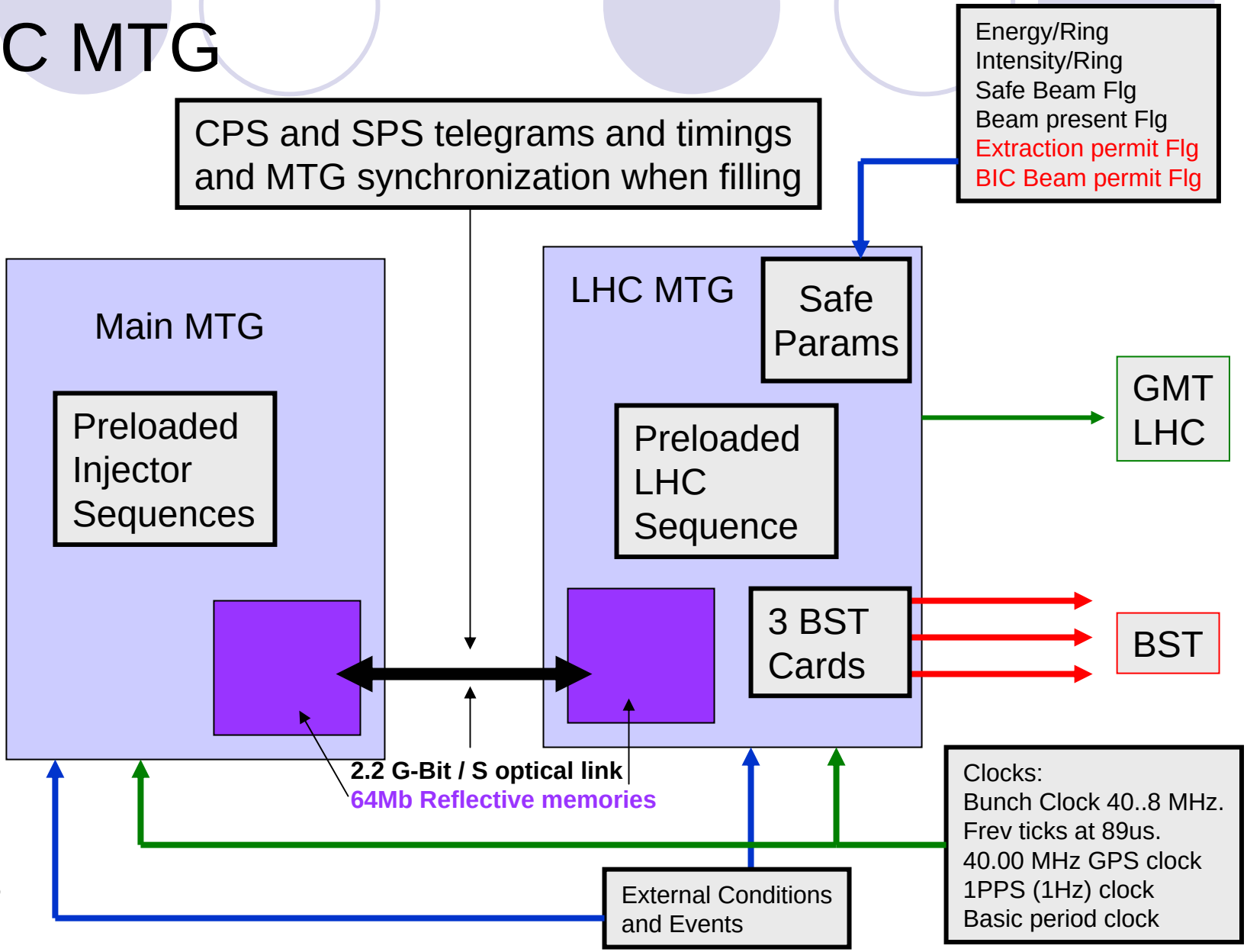
Overview I
Central Timing. What's the CBCM ?

- The Central Beam and Cycle Manager CBCM (7 VME Crates + Two racks of equipment) is a collection of hardware and software systems responsible for coordinating and piloting the timing systems of CERN's accelerators.
- In the LHC era, the CBCM will control Linac-II, Linac-III, the PSB, CPS, ADE, LEI, SPS and the LHC timing systems. The CTF, although piloted using a similar system, runs on its own, on a completely separated timing network.
- The CBCM will also drive the Beam Synchronous Timing (BST) for LHC. There will be 3 distributions R1, R2, Experiments.

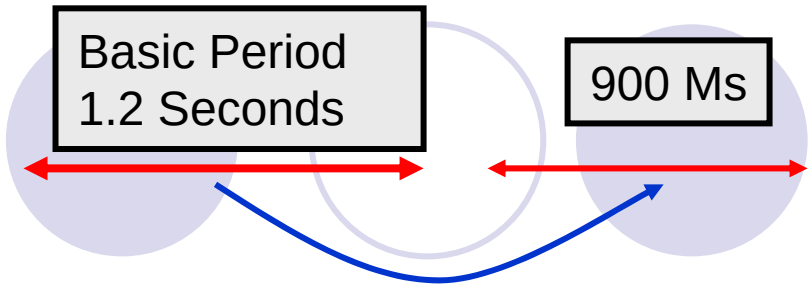
Overview II
Central Timing

- The LHC machine timing must be closely coupled with the injector chain during the filling process, but once the fill has completed, the LHC is independent from its injector chain.
- The LHC central timing will be implemented on independent hardware with 2.2G-bit/S reflective memory data link to central MTG.
- Once filled, the link is partially closed, effectively isolating the LHC from its injector chain. There will still be some other timing events from SPS to be forwarded on the LHC timing cable.

Hardware II
LHC MTG



Overview III
Central Timing



- Almost certainly the basic period in the LHC era will have been reduced from its current value of 1.2S to 900ms. All cycles of all machines are composed of basic periods, and injections into the LHC from the SPS will occur at multiples of a basic period apart.
- The CBCM transmits the UTC time 100us early so that transmission time delays can be compensated for at the receiver cards. The transmission time delay is corrected in the CTR via a 40MHz clock recovered by an onboard hybrid PLL.
- Hence time stamps can have better than 25ns precision, less than 10ns jitter, and 1ns resolution.

Hardware I
Clock and UTC time generation

GPS

GPS
One pulse
per Second

Smart clock
PLL

PLL
One pulse
per Second

Phase locked
10MHz

CTSYNC

40MHz PLL

Basic Period
1200/900/600 ms

Advanced (100us)
One pulse
per Second

Synchronized 1KHz
(slow timing clock)

Phase locked
10MHz

Control System

Phase looked
40 MHz Event
encoding clock

Event
tables

CTGU

The
new
generation
low
jitter <1ns
VME
based
MTG
module

RS485
Timing

CERN
UTC
Time

RS485
Timing

CERN
UTC
Time

Timing receiver

40 MHz

10 MHz

Delay

CTRP

1 KHz

1PPS

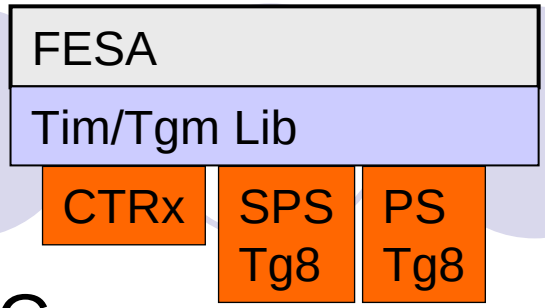
25ns steps

Set once on startup
& on Leap Seconds

UTC time (NTP or GPS)

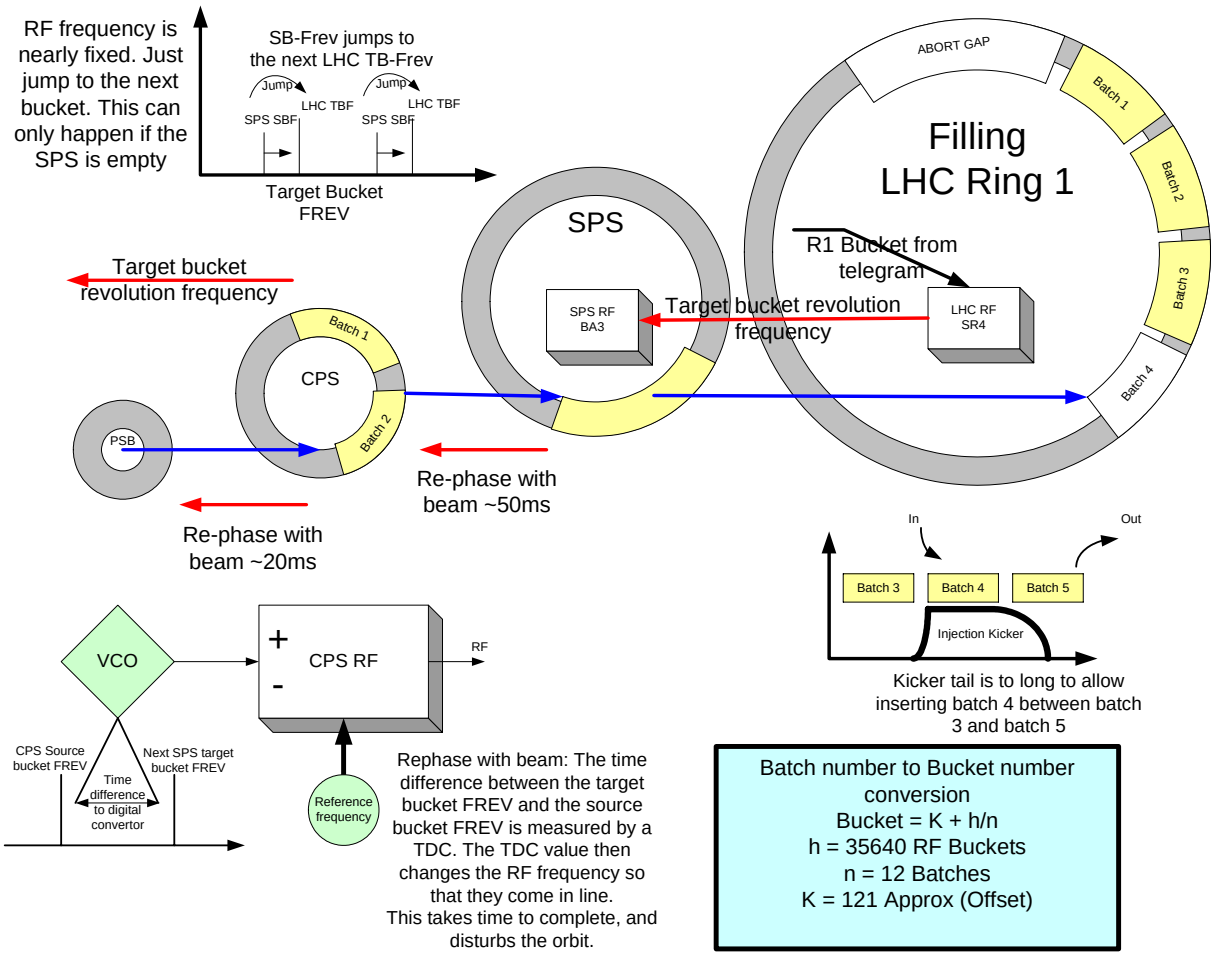
External events

Overview IV
Timing Reception

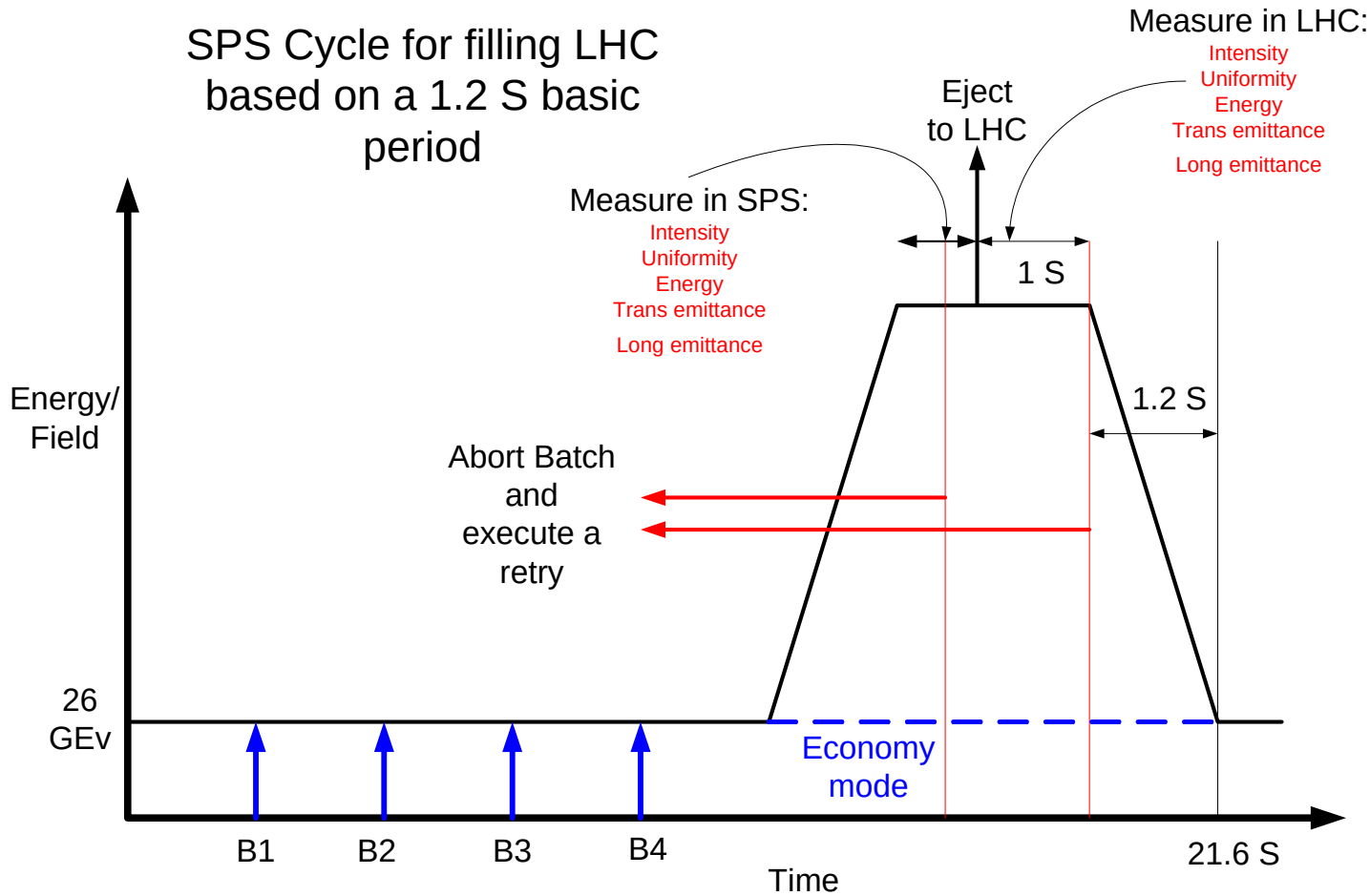


- The CTRx V/VME I/PCI P/PMC
- Down to 1ns UTC time stamping if HPTDC installed, else 25ns
- 50MHz external clocks
- 1PPS 1KHz 10MHz and 40MHz internal clocks
- Counters are 24-bit
- 2048 actions supporting MP and PPM
- Telegram and Payload handling
- Full counter remote control
- Fully Integrated into FESA, Alarms monitor

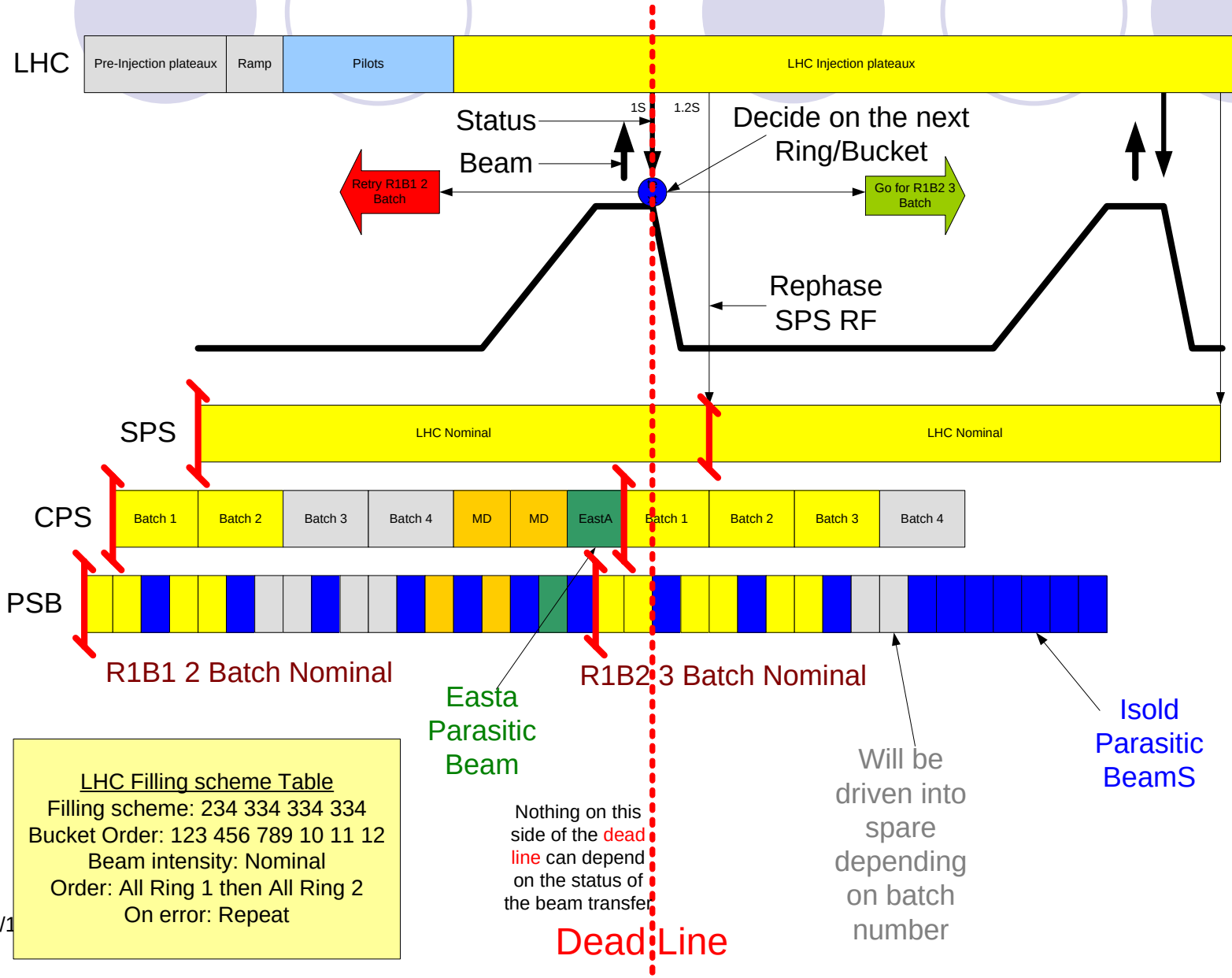
RF synchronization



Go no Go and retries



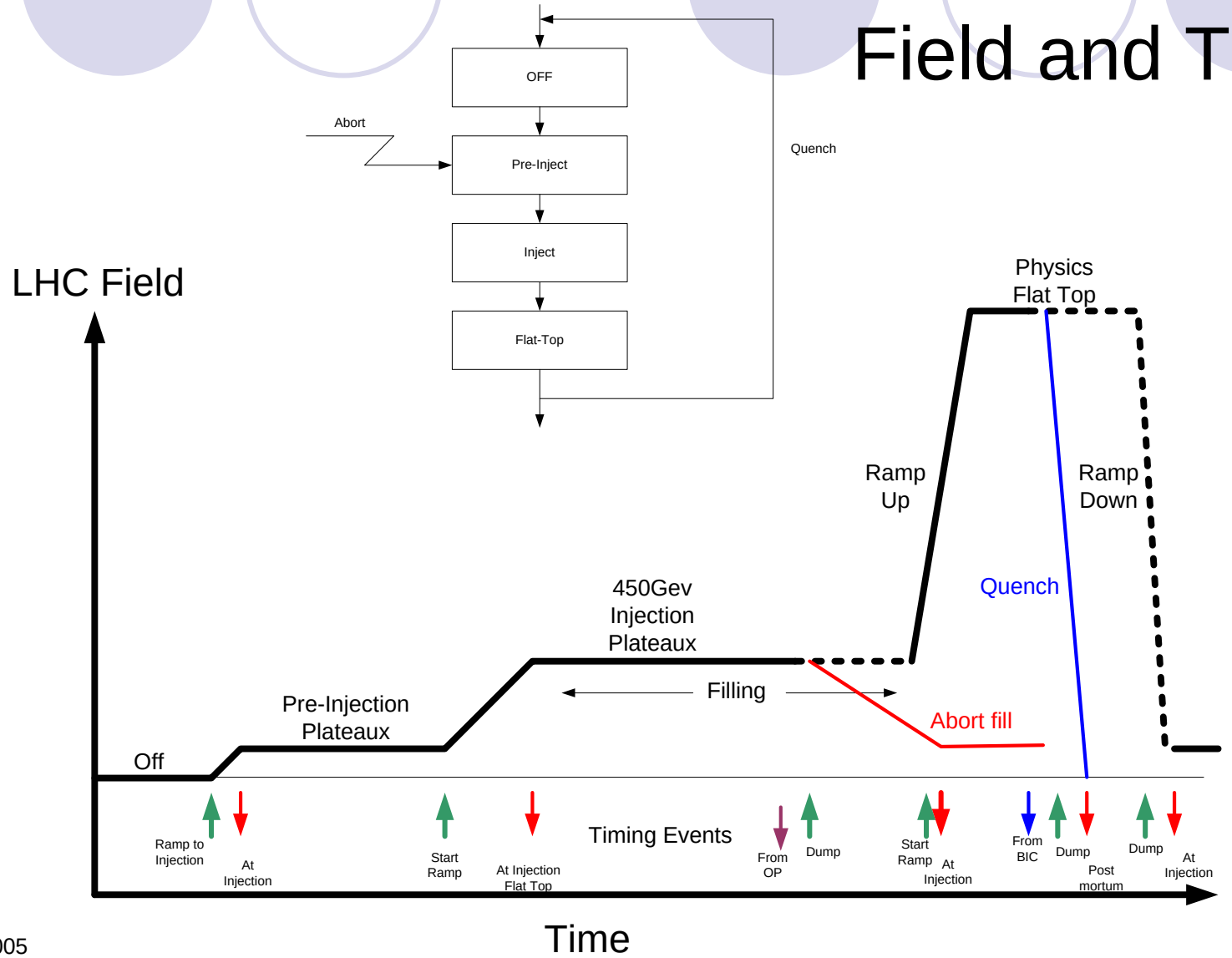
LHC Filling



LHC Filling scheme Table
Filling scheme: 234 334 334 334
Bucket Order: 123 456 789 10 11 12
Beam intensity: Nominal
Order: All Ring 1 then All Ring 2
On error: Repeat

There is still a lot of discussion needed to precisely define the interaction between the central timing, operations, power supplies, BIC, and monitoring applications

Field and Timing



LHC Timing cable

- The LHC telegram which will contain at least the following information: 0x14xxyyyy
  - USER: The cycle ID, it has values like PILOT, NOMINAL, DUMP MD…
  - PARTY1: The particle type in Ring-1, Protons/Ions from LEIR
  - PARTY2: The particle type in Ring-2
  - FIELD: Related to the Beam Energy (Units of 10Gs fits 16 Bits 10T=10000x10Gs)
  - INTEN1: The Beam Intensity in Ring-1 (Units ?)
  - INTEN2: The Beam Intensity in Ring-2 (Units ?)
  - RING: The next ring to be injected Ring-1, Ring-2, NONE
  - BUNCH: The next target bunch position in the ring 0..35640
  - BATCH: The actual batch number in the ring 1..12
  - BATCHES: The number of CPS batches
  - MODE: The machine mode, Pre-injection, Injection, Ramping, Physics, DUMP etc (Need a list)
  - BPNM: The basic period number from the start of the cycle
  - COMLN: Timing trigger bit patterns which are calculated by the CBCM to trigger specific actions.
  - STATUS: Machine status bits like, OK, ABORT, QUENCH
  - BEAMID: Identifies the next beam in all injectors
- The SPS telegram
- The CPS telegram
- The UTC time each second
- The LHC 1KHz events 0x0100xxxx
- The LHC machine events CTIM X:=: 0x13xx0000
- Some CPS & SPS events such as the SPS extraction kicker warning pre-pulse.

Can have NO "next" lines

Event Type = 3

CTIM X = F (code)

Payloads = 0000 for LHC events

LHC Machine = 1

External conditions and events

- An external condition is a logic level that must remain set long enough for the CBCM to poll it.. They represent interlocks and operator requests. The CBCM responds slowly to these conditions, typically within a few seconds. They can be presented to the CBCM on cables or by software, and they control sequence switching, normal/spare, and other functions such as for the Linac tail clipper, and batch logic.
  - Example SPS-Proton-Request
  - MPS Down ….
- An external event is an edge presented directly to the CTG, a corresponding action, (usually send out an event), occurs within 2ms.
  - Example Start-Flat-Top
  - Dump beam
  - Post Mortem …..

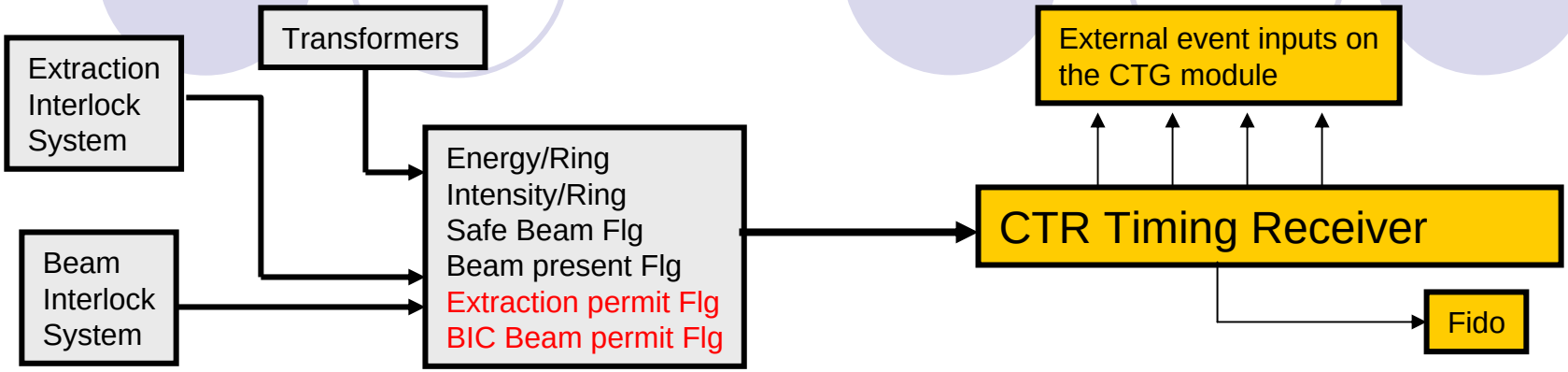
LHC External Conditions

- MPS-Ready
- On Pre-Injection plateaux
- On Injection plateaux
- On Physics plateaux
- Protons circulating Ring-1/Ring-2
- Request high intensity
- Request low intensity
- Abort fill
- BIC Beam Permit R1
- BIC Beam Permit R2
- Extraction Permit
- SPS bad beam parameters
- LHC bad beam parameters

In general the **more interlocks** supplied to the CBCM, the **better the diagnostic** we get for why the system is executing the beam it is. For example for a given beam destination X, say a certain septum magnet Y must have a good status, and a certain operator request must be present. In this case, if the septum is down, the CBCM will try to choose another beam to execute, and provide the diagnostic, *"That beam couldn't be executed because the destination was X and septum Y was down."* However if the operator request and the septum magnet status were combined into a single bit, then it would be impossible to tell the difference between a faulty septum and no request for beam being present.

The more **interlocks** we have, the **smarter the CBCM behavior** can be because it knows the cycle composition in advance, and can take action BEFORE the cycle starts execution.

Safe Beam parameters



Some of these parameters look like external conditions, some transitions will trigger external events. Others like the Beam Energy and Intensity per ring are sent out over the GMT and BST cables at regular intervals.

The encoding for these parameters will be the same as on the GMT so that they can be received in a straight forward way using a CTR and the standard driver. CTR outputs can trigger external events by directly driving the CTG external event inputs.

There are other interlock systems we need information from, such as the extraction interlocks, and it would be very nice if the Extraction permit flag was also sent over the Safe Beam system

LHC External events

- DUMP
- BIC Interlock down
- POST Mortem
- Commit changes

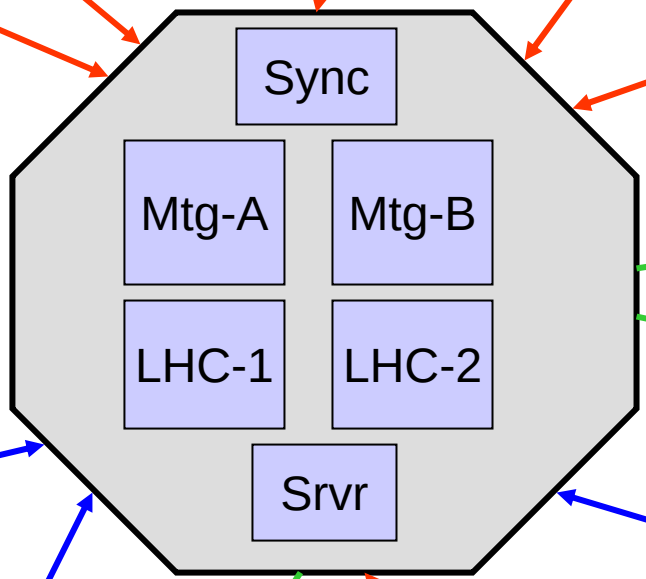
Emergency actions where we need to get an event out fast. This behavior is handled directly in the CTG card by hardware. In fact any pre-loaded CTG program can be executed on reception of an external event

LHC Events

- Ramp up to Pre-inject
- Ramp up to Inject
- Ramp up to Physics
- Dump
- At Pre-Inject
- At Inject
- At Physics
- Abort fill
- BIC Interlock down
- Ramp down to Pre-Inject
- Post mortem
- Commit changes
- Start basic period
- LHC Telegram ready
- Acquire acquisition data
- … …

Events and Telegrams from other machines can be routed across the LHC/Main MTG data link using the reflective memory. There will certainly be some SPS and CPS events/telegrams on the LHC timing cable.

CBCM Context Diagram



SPS Interlocks
LHC Extraction Permit
SPS bad beam parameters
EDF, P+ Rq

LHC Beam parameters
Field Strength/Energy
Intensity R1, R2

GMT Clocks
1PPS, 40.0MHz
Basic-Period
UTC Time

LHC Interlocks
MPS-Ready
On Pre-Injection plateaux
On Injection plateaux
On Physics plateaux
Protons circulating Ring-1/Ring-2
Request high intensity
Request low intensity
Abort fill
BIC Beam Permit R1
BIC Beam Permit R2
LHC bad beam parameters

BST Clocks
BC R1 R2 Exp
FREV

GMT Cables
LEI,PSB,CPS,
ADE,SPS,LHC

BST Cables
R1,R2,Exp

External Events
CPS ELFT….
SPS Commit
LHC Commit
LHC Dump
LHC Post Mortem

HW External Conditions
96 assorted interlocks
Inhibits and Requests

Alarms
HW & SW Status

Volatile Interlock Logic
Normal/Spare
Sequence Change
Cycle Building

Middle Ware
SW External conditions
Timings CTIM
Sequences
BCDs, Beams, Cycles
LHC Filling Scheme